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10EC71

Seventh Semester B.E. Degree Examination, June/July 2015
Computer Communication Networks

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Mention the layers of TCP/IP protocol suite and give brief explanation of protocols used in the suite. (10 Marks)
- b. Explain usage of existing loops, adaptive technology and discrete multitone technique in ADSL. (10 Marks)
- 2 a. Give design of selective repeat ARQ, and explain its working at sender site and receiver site. (10 Marks)
- b. Give frame format of HDLC protocol and explain all the fields in the frame. (10 Marks)
- 3 a. Explain working of CSMA/CA with a flow diagram. (10 Marks)
- b. A pure aloha network transmits 200 bit frames on a shared channel of 200 kbps. What is the through put if system produces 1000 frames per second? (04 Marks)
- c. Explain the idea of CDMA technique. (06 Marks)
- 4 a. Explain frame format of Ethernet MAC frame. (08 Marks)
- b. Describe topology, implementation and encoding in fast ethernet. (08 Marks)
- c. Give summary of standard ethernet implementations. (04 Marks)

PART – B

- 5 a. Describe the three steps involved in finding spanning tree for the following system Fig. Q5 (a). (10 Marks)

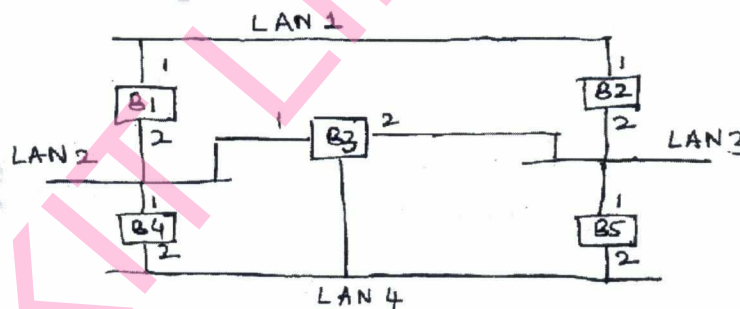


Fig. Q5 (a)

- b. Discuss the two most common architectures in backbone networks. (10 Marks)
- 6 a. Explain classful addressing classes in IPV4. (10 Marks)
- b. Explain the different fields of IPV₄ datagram. (10 Marks)
- 7 a. Explain initialization, sharing and updating in distance vector routing protocol. (10 Marks)
- b. Discuss multicast distance vector routing and its implementation in DVMRP. (10 Marks)
- 8 a. Explain UDP datagram format. (04 Marks)
- b. Describe three way hand shaking connection establishment and termination in TCP. (08 Marks)
- c. Mention atleast five generic and country domains and explain recursive and iterative resolution. (08 Marks)

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
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Seventh Semester B.E. Degree Examination, June/July 2015
Optical Fiber Communication

Time: 3 hrs.

Max. Marks:100

**Note: 1. Answer any FIVE full questions, selecting
atleast TWO questions from each part.
2. Missing data may be suitably assumed.**

PART – A

1.
 - a. With neat block schematic explain the working of an optical fiber transmission link? Briefly explain the characteristics and operating ranges of a key optical fiber link components. (10 Marks)
 - b. Design a single mode guide for operating at $\lambda = 1.3\mu\text{m}$ with fused silica core $n_1 = 1.458$ with $\text{NA} = 0.3$. Specify n_2 and "a" for the mode. Will the guide still be single mode if $\lambda = 0.82\mu\text{m}$. If not how many modes will exist. (04 Marks)
 - c. With neat sketches, explain with reference to ray optics
 - i) NA
 - ii) Skew rays
 - iii) Acceptance angle. (06 Marks)
2.
 - a. Explain the following parameters: i) Absorption; ii) Group delay; iii) Scattering loss; iv) Chromatic dispersion; v) Bending loss. (10 Marks)
 - b. The mean optical power launched into an optical fiber link is 1.8mw and the fiber attenuation is 1.8dB. Determine the maximum possible link length without repeaters when the minimum optical power level required at detector is $4\mu\text{W}$. Calculate the power received in dBm after 10km. (04 Marks)
 - c. Describe and explain signal distortion in optical fibers. (06 Marks)
3.
 - a. With neat sketches, explain the characteristics and function of the double hetero structure device. (06 Marks)
 - b. A double heterojunction InGaAsP. LED emitting a peak wave length of 1310nm has radiative and non radiative recombination times of 30 and 100ns respectively. The drive current is 40mA. Calculate the bulk recombination life time, internal quantum efficiency, internal power level. (04 Marks)
 - c. Compare the operating characteristics of the Si, Ge and InGaAs with PIN and APD diodes. (06 Marks)
 - d. A silicon APD has a quantum efficiency of 75% at a wavelength of 900nm. Suppose $0.8\mu\text{W}$ of optical power produce a multiplied photocurrent of $10\mu\text{A}$. Find the multiplication factor. (04 Marks)
4.
 - a. Explain the function of a good connector? With neat sketches, explain the biconical ferrule connector. (06 Marks)
 - b. A four port multipart fiber FBT coupler has $60\mu\text{W}$ optical power launched into port 1. The measured output power at ports 2, 3 and 4 are 0.004, 26.0 and $27.5\mu\text{W}$ respectively. Determine the excess loss, the insertion loss between the input and the output ports, the cross talk and the split ratio of the device. (04 Marks)
 - c. With neat sketches, explain the role and types of splicing techniques used in OFC. (06 Marks)
 - d. A GIF has a parabolic RI ($\alpha = 2$) and a core diameter of $50\mu\text{m}$. Estimate the insertion loss due to a $3\mu\text{m}$ lateral misalignment at a fiber joint when there is index matching and assign
 - i) Uniform illumination of all guided modes only
 - ii) Uniform illumination of all guided modes and leaky modes. (04 Marks)

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PART – B

- 5 a. With neat sketches, explain the power full measurement tools for accessing the data handling ability of a digital transmission system. (08 Marks)
- b. Explain the various noise and disturbance associated with the signal detection system. (06 Marks)
- c. Write a note on analog receiver. (06 Marks)
- 6 a. With neat sketches explain the optical power loss model for a point to point link. (08 Marks)
- b. Explain the basic elements of an analog link and the major noise contribution. (08 Marks)
- c. Explain the basic concept of sub carrier multiplexing. (04 Marks)
- 7 a. Explain the concept and basic tuning option of a tunable lasers and depict the relation between tuning range, channel spacing and source spectral width. (06 Marks)
- b. Explain the operation of 4×4 OADM. (04 Marks)
- c. Explain the operation of Etalon. Design 4 channel multiplexing using TTF. (10 Marks)
- 8 a. Explain the possible applications of optical amplifier. (04 Marks)
- b. With neat sketches, explain the simplifier energy level and various transition process of Er^{3+} in silica. (06 Marks)
- c. Explain the basic formats of STS N sonnet frame and STM-N-SDH frame. (05 Marks)
- d. Write a note on high speed light wave links. (05 Marks)

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Seventh Semester B.E. Degree Examination, June/July 2015
Power Electronics

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

1.
 - a. What is power electronics? State the applications of power electronics. (06 Marks)
 - b. Give symbol, characteristics features of the following devices:
i) IGBT ii) TRIAC iii) GTO iv) MCT. (08 Marks)
 - c. What are the peripheral effects of power electronic equipments and mention the remedies. (06 Marks)

2.
 - a. Compare IGBT, MOSFET and BJT's. (04 Marks)
 - b. What is the need of a base drive control in a power transistor? Explain proportional and anti-saturation control. (08 Marks)
 - c. With the necessary waveforms, explain the switching characteristics of a power MOSFET. (08 Marks)

3.
 - a. Explain the two transistor model of SCR and derive the formula

$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$
 (06 Marks)
 - b. With a neat sketch, explain turn-off characteristics of SCR. (06 Marks)
 - c. Design the snubber circuit elements R_S and C_S connected across the SCR, given that
 $\frac{dv}{dt}(\max) = 180V/\mu s$ and $\frac{di}{dt}(\max) = 45A/\mu s$. An inductor $L = 0.1H$ and a resistance $R \ll R_S$ are in series with the SCR with a 300V, DC applied to the circuit. (08 Marks)

4.
 - a. With a neat diagram and waveforms, explain the principle of single phase full converter purely resistive load. Derive the expression for voltage output and rms output voltage. (10 Marks)
 - b. For the converter shown in Fig.Q.4(b) has a purely resistive load of R and the delay angle is $\alpha = \pi/2$ determine: i) the rectification efficiency; ii) the form factor; iii) ripple factor (RF); iv) the TUF; v) PIV of thyristor. (10 Marks)

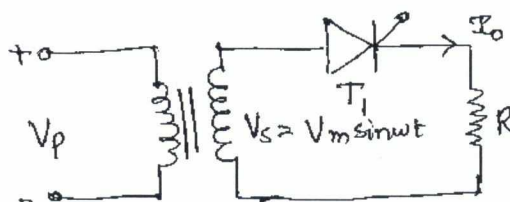


Fig.Q.4(b)

PART – B

- 5 a. Explain the self commutation with the help of neat sketch and obtain the expression for the capacitor voltage and current. (08 Marks)
- b. Compare natural and forced commutation. (04 Marks)
- c. With the necessary circuit diagram and waveforms, explain the operation of a complimentary commutation. (08 Marks)
- 6 a. What are the application of AC voltage controller? (04 Marks)
- b. With the help of circuit diagram explain the operation of single phase AC regulator using ON-OFF control. Derive the expression for rms value of load voltage. (08 Marks)
- c. A single phase AC voltage controller with R-L load has the following details. Supply voltage = 230V, 50Hz, $R = 4\Omega$ and $WL = 3\Omega$, calculate:
- The control range of firing angle.
 - The maximum value of RMS load current.
 - The maximum power and power factor.
 - The maximum values of average and RMS thyristor current. (08 Marks)
- 7 a. Give the classification of choppers. Explain class E-chopper with circuit and quadrant diagram. (06 Marks)
- b. With the help of neat circuit diagram and waveforms. Explain the working principle of a step-up chopper. (06 Marks)
- c. A step down chopper is operating at a frequency at 2kHz from a 250V dc source to supply a load resistance of 12Ω . The time constant of the load circuit is 10ms. If the average load voltage is 150V, calculate: i) The ON-time t_{ON} of the chopper; ii) The average and rms values of load current and iii) the peak to peak ripple current. (08 Marks)
- 8 a. What do you mean by inverters? Explain the principle operation of 1- ϕ half bridge inverter. (08 Marks)
- b. Write and explain the performance parameter of an inverter. (06 Marks)
- c. With a neat, circuit diagram explain the variable DC link inverter. (06 Marks)

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Seventh Semester B.E. Degree Examination, June/July 2015
Embedded System Design

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

- 1
 - a. Explain the major elements of an embedded system design and development process with a suitable schematic. **(08 Marks)**
 - b. Discuss the basic computing engines of an embedded system with suitable diagrams for each. **(07 Marks)**
 - c. Write an explanatory note on finite state machine model. **(05 Marks)**
- 2
 - a. Discuss how an error can be propagated in the numbers representations. Explain with an example. **(06 Marks)**
 - b. What are the various addressing modes in an instruction? Explain each with an example. **(07 Marks)**
 - c. Briefly explain the concept of an execution flow of an instruction in an embedded application. **(07 Marks)**
- 3
 - a. List and explain the various types of memory. **(06 Marks)**
 - b. With a neat diagram, explain the design of a $4K \times 16$ SRAM system. **(08 Marks)**
 - c. Explain the following: i) Swapping ii) Overlays. **(06 Marks)**
- 4
 - a. Briefly explain the common life cycle models of an embedded systems with a suitable diagrams for each. **(08 Marks)**
 - b. Discuss the system design specifications in an embedded systems with an example. **(08 Marks)**
 - c. Enumerate the difference between functional model and architectural model. **(04 Marks)**

PART – B

- 5
 - a. What is a thread? Explain the different types of threads used in an operating system. **(06 Marks)**
 - b. List the different types of operating system services and explain them briefly. Also, discuss the significance of the architecture of an operating systems. **(08 Marks)**
 - c. With a suitable schematic and program, explain the task control block. **(06 Marks)**
- 6
 - a. Explain the different types of stacks used in the memory management. **(06 Marks)**
 - b. Discuss the significance of duplicate hardware context with a suitable diagram. **(06 Marks)**
 - c. With a suitable code, explain how a simple Kernel will be developed. **(08 Marks)**
- 7
 - a. Explain the purpose of the complexity analysis by suggesting a suitable algorithm for that. **(07 Marks)**
 - b. With suitable examples, explain how the comparison of algorithms can be done. **(06 Marks)**
 - c. Discuss the design of a memory map used in memory loading, with an example. **(07 Marks)**
- 8
 - a. With suitable algorithms, explain the analysis of search and sort to determine their complexity. **(08 Marks)**
 - b. What is time loading? Explain the primary methods used to compute the times. **(06 Marks)**
 - c. Explain the following: i) Polled loops ii) Co-routine. **(06 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2015
DSP Algorithm and Architecture

Time: 3 hrs.

Max. Marks: 100

**Note: Answer any FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

1.
 - a. With neat block diagram, explain digital signal processing system. (04 Marks)
 - b. Explain common features of programmable digital signal processor. (08 Marks)
 - c. Explain decimation and interpolation process. (08 Marks)

2.
 - a. Write the structure of 4×4 Braun multiplier and explain its concept. (06 Marks)
 - b. It is required to find sum of 256 numbers each is represented by 16 bits. How many bits should the accumulator have so that the sum is computed without overflow? It is decided to have a accumulator with 16 bits, by how many bits each number is shifted to avoid overflow? (04 Marks)
 - c. With the help of block diagram, explain program sequencer. (06 Marks)
 - d. Write the block diagram of parallel implementation of 8 – tap FIR filter using two MAC units. (04 Marks)

3.
 - a. With neat diagram,, explain barrel shifter of TMS320C54XX processor. (05 Marks)
 - b. With the help of block diagram, explain direct addressing mode of TMS320C54XX processor. (05 Marks)
 - c. The register AR4 with contents 1010H is selected as pointer for circular buffer. If circular buffer size is 48, what would be loaded into circular buffer size (BK) register? Determine start address and end-address of buffer. What would be the contents of AR4 after execution of the instruction *AR4 + 0%, A, if contents of AR0 register is 0025H? (05 Marks)
 - d. Explain processor mode status (PMST) register of TMS320C54XX processor. (05 Marks)

4.
 - a. Describe the operation of following instructions :
 - i) MAC *AR3 –, *AR4 +, B, A
 - ii) MPY *AR5 –, *AR4 + 0, B
 - iii) RPT #8. (06 Marks)
 - b. Show the pipeline operation of following sequence of instructions, if initial value of AR1, AR3, and A are 84, 81, 1 and value stored in memory locations 81, 82, 83, 84 are 2, 3, 4, 6. Also provide values of registers AR3, AR1, A after completion of each cycle.

ADD *AR3 +, A
 LD *AR1+, T
 MPY *AR3+, B
 ADD B, A. (08 Marks)
 - c. With the help of logical block diagram, explain hardware timer circuit. (06 Marks)

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PART – B

- 5 a. Represent both $N_1 = 0.5$ and $N_2 = 0.25$ in Q15 number notation and write assembly language program for TMS320C54XX processor to multiply obtained Q15 numbers. (06 Marks)
- b. Determine the value of each of the following 16-bits numbers represented using Q-notation.
- 4400h as a Q7 number
 - 4400h as a Q0 number
 - 2ccch as a Q15 number
 - E6EFh as a Q15 number. (04 Marks)
- c. Show the memory organization for digital interpolation using 15 tap FIR filter with interpolation factor 5. (04 Marks)
- d. What is the drawback of linear interpolation filter? Explain the scheme to overcome this drawback. (06 Marks)
- 6 a. Why scaling is required before or during butterfly computation? Draw the butterfly computation that uses 0.25 as scale factor. (04 Marks)
- b. Determine the following for a 128 point FFT computation :
- Number of stages
 - Number of butterflies in each stage. (02 Marks)
- c. With an example, explain bit reversed index generation in TMS320C54XX DSP. (08 Marks)
- d. Write the subroutine program to find the spectrum transformed data using TMS320C54XX DSP. (06 Marks)
- 7 a. With neat timing diagram, explain external memory interface singles of TMS320C54XX processor for read-read-write operations. (10 Marks)
- b. Discuss the interrupt handling in TMS320C54XX processor. (10 Marks)
- 8 a. With the help of block diagram, explain synchronous serial interface between TMS320C54XX and CODEC. (04 Marks)
- b. Explain the building blocks of PCM3002 CODEC. (08 Marks)
- c. With the help of block diagram, explain JPEG algorithm. (08 Marks)

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10EC762/10TE762

Seventh Semester B.E. Degree Examination, June/July 2015
Real Time Systems

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1 a. How are RTS classified based on time constraint? Explain them with an example and appropriate equations. (08 Marks)
- b. Explain periodic and aperiodic tasks with examples. (06 Marks)
- c. Discuss the different types of programs in system design. (06 Marks)
- 2 a. What do you mean by inferential control? Draw general structure of inferential control configuration. Explain inferential control by taking the example of binary distillation column. (08 Marks)
- b. Explain the following :
i) Batch process and continuous process. ii) PID control algorithm (08 Marks)
- c. Write a note on distributed systems. (04 Marks)
- 3 a. Explain Analog input and Analog output system with neat block diagrams. (10 Marks)
- b. With help of neat diagrams. Explain working principle of Daisy-Chain interrupt structure. (06 Marks)
- c. Explain Asynchronous and synchronous transmission techniques. (04 Marks)
- 4 a. Explain the following with respect to real time programming language.
i) Portability ii) Global and local variables iii) Derived types iv) Coroutines (08 Marks)
- b. Discuss control structures used in Real Time programming languages. Write neat diagrams of standard structured program constructs. (06 Marks)
- c. How Interrupts and Device Handling operations performed in Real time programming languages. (06 Marks)

PART – B

- 5 a. Explain Multi-user and Multi-tasking operating system with suitable diagrams. (08 Marks)
- b. What are the two scheduling strategies? Explain briefly. (05 Marks)
- c. What are the functions of a task management module? Explain various tasks states with the help of a state diagram. (07 Marks)
- 6 a. What is code sharing? Explain the serially reusable and recetrant code. (07 Marks)
- b. What is binary semaphore? Explain function of binary semaphore by considering a task which wishes to access a printer. (08 Marks)
- c. Write a note on minimum operating system Kernel. (05 Marks)
- 7 a. Explain planning phase and development phase involved in the design of a RTS. (10 Marks)
- b. Write the flow chart for a single program approach. (05 Marks)
- c. Write a note on the basic software module, with respect to RTS. (05 Marks)
- 8 a. Show the outline of abstract modeling approach of ward and mellor method and explain. (10 Marks)
- b. Draw state transition matrix for drying over in case of ward and mellor method. (05 Marks)
- c. Explain architecture model with neat diagram in case of Hately and Pirbhai Mehtod. (05 Marks)

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